IN THE CLAIMS:

1. A multiple-channel semiconductor device, comprising:

a first insulator layer on a substrate;

a first channel region on the first insulator layer;

a second insulator layer on the first channel region;

a second channel region on the second insulator layer;

a third insulator layer on the second channel region; and

a gate electrode on the third insulator layer.

2. The device of claim 1, wherein the first and second channel regions are lightly doped with a first conductivity type of dopant.

3. The device of claim 2, wherein the gate electrode is heavily doped with a second conductivity type of dopant different than the first conductivity type.

4. The device of claim 3, wherein the first and second channel regions and the gate electrode are doped silicon.

5. The device of claim 4, further comprising doped silicon spacers on the substrate and forming sidewall spacers contacting the first and second channel regions.

6. The device of claim 5, further comprising thermal oxide on sidewalls of the gate electrode.

7. The device of claim 5, further comprising CVD oxide on sidewalls of the gate electrode.

8. The device of claim 4, further comprising raised source and drain regions on the substrate and contacting the first and second channel regions.

9. The device of claim 1, wherein the insulator layers are oxide.

10. The device of claim 1, wherein at least one of the insulator layers is a high K gate dielectric.

11. The device of claim 1 wherein the channel regions are SiGe.

12. The device of claim 1, wherein the gate electrode is doped SiGe.

13. The device of claim 1, wherein the gate electrode is at least one of a metal or a silicide.

14. A method of forming a multiple-channel semiconductor device, comprising the steps:

forming a stack on a substrate, the stack including at least two lightly doped channel regions vertically separated from each other and from the substrate by insulator layers, and a gate electrode separated from the channel regions by an insulator layer;

forming an oxide liner on sidewalls of the gate electrode;

forming source and drain regions contacting sidewalls of the channel regions; and

forming gate electrode spacers on the oxide liner on the gate electrode.

15. The method of claim 14, wherein the step of forming an oxide liner includes forming a thermal oxide liner on the sidewalls of the gate electrode.

16. The method of claim 15, wherein the step of forming gate electrode spacers on the oxide liner include depositing nitride on the oxide liner and the gate electrode and performing a spacer etch stopping on the insulator layer separating the gate electrode from the channel regions.

17. The method of claim 16, wherein the step of forming a stack includes dry etching the insulator layers and the channel regions after the gate electrode spacers are formed, stopping the dry etching on the insulator layer separating the channel regions from the substrate.

18. The method of claim 17, further comprising implanting source and drain extensions into the substrate after the dry etching.

19. The method of claim 18, wherein the step of forming source and drain regions includes depositing a lightly doped semiconductor layer over the stack and the gate electrode spacers after the implanting of the source and drain extensions, and depositing a heavily doped semiconductor layer over the lightly doped semiconductor layer.

20. The method of claim 19, wherein the step of forming source and drain regions further includes dry etching the lightly doped and heavily doped semiconductor layers to form semiconductor spacers on the sidewalls of the channel regions.

21. The method of claim 20, further comprising forming device spacers on the semiconductor spacers and performing a service and drain implantation into the substrate with the device spacers masking the source and drain extensions.